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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	
FOLMSBEE, Alan C.	Docket No. SUNMP210
Application No. 09/376,654	Examiner: Benjamin E. Lanier
Filed: August 18, 1999	Group Art Unit: 2132
For: Secure Program Execution Depending On Predictable Error Correction	Date: January 5, 2007
	Confirmation No. 6747

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on January 5, 2007.

Signed: _____
Sylvia Castillo

REPLY BRIEF

Mail Stop: **APPEAL BRIEF – PATENTS**
Honorable Commissioner for Patents
Alexandria VA 22313-1450

Dear Sir:

In response to the Examiner's Answer of November 7, 2006, Appellant respectfully submits the present Reply Brief in accordance with 37 C.F.R. § 41.41. Since the two-month period for submitting a Reply Brief expires January 8, 2007, the present Reply Brief is timely. Please consider this Reply Brief, in which:

Remarks begin on page 2 of this paper.

REMARKS

Appellant will limit comments herein specifically to points raised by the Examiner in the "Response to Arguments" section of the Examiner's Answer. Each point discussed in the Examiner's Answer is addressed under a separate heading below, which identifies the location of the point raised by the Examiner, and a brief description.

Examiner Answer, paragraph bridging pages 6-7: ***On whether Chen discloses RAM on the chip...***

The Examiner suggests in the paragraph bridging pages 6 and 7 of the Examiner's Answer that the Intel Pentium Pro processor mentioned by Chen has "RAM on said chip storing error correcting information, said RAM being in communication with said programmable error correcting circuit" as set forth in claim 1 ("Chen" referring to the primary reference, U.S. Patent 6,044,483). It being noted also, that claim 1 requires that the programmable error correcting circuit generates corrected processor instructions in response to the processor instructions containing errors and the error correcting information stored in the RAM.

With regard to the Examiner's remarks, the Appellant is confused as to whether the prior art being asserted against the claims is Chen, the Pentium Pro processor, or some combination thereof. Specifically, the Examiner seems to have gone beyond the scope of Chen in putting forth his argument that Chen anticipates the claim limitations. See, for example, the figure on page 7 of the Examiner's Answer.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (emphasis added). The Examiner appears to be arguing that the Pentium Pro processor referred to in Chen has some features, described on page 7 of the Examiner's Answer, without offering any proof that those features are present. However, 35 U.S.C. § 102, each and every element as set forth in the claim must be described in the single prior art reference.

Now, it is possible that the Examiner is suggesting that Chen inherently discloses that the ECC support provided in the Intel Pentium Pro includes an ECC circuit on the processor chip, and not on a separate chip in the same package, or in external chips. (The Pentium Pro

is, in fact, a multi-chip module having a processor on one chip, an L2 cache on separate chips, as well as a separate "chip set" external to the module.[1]) Any of these chips aside from the one having processing circuitry, could have the error correcting logic. Therefore, the Examiner's assumption regarding the Pentium Pro processor is not justified by what is disclosed by Chen. As is made plain in the disclosure, it is a feature of the present invention that the error correcting logic be on the same chip as the processor, combining the two functions on a single chip makes it more difficult for a person to obtain a clean copy of the software (i.e., software without the errors inserted therein). That is, they cannot simply probe the connections to the processor itself to obtain the instructions sans any inserted errors. Chen does not show a microprocessor having error-correcting circuit on the same chip as the processing circuitry as claimed.

Appellant recognizes that express, implicit, and *inherent* disclosures of a prior art reference may be relied upon in the rejection of claims under 35 U.S.C. § 102. However, the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. See MPEP 2112 IV. "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is ***necessarily present*** in the thing described in the reference, and that it would be so recognized by persons of ordinary skill" (*In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981) (emphasis added). Appellant respectfully submits that the Examiner has not met the burden of proving that the missing descriptive matter is necessarily present in Chen, and therefore, Chen does not anticipate the claim.

Finally, the Examiner makes the assertion that, "These registers [in a simple processor] can be considered RAM because they are volatile data storage modules" (page 7, first line of text). Appellant disagrees. RAM is a well-known acronym that stands for "Random Access Memory." RAM therefore requires that the memory can be accessed at random. Furthermore, there is no requirement that RAM be volatile. Flash RAM, the type of memory used in USB thumb-drives and digital cameras, is not volatile since it maintains the data even when disconnected from any power source. There is no suggestion that the registers described by the Examiner as existing in the Pentium Pro processor are randomly accessible. Since they are not randomly accessible, they are not addressable, and therefore are not RAM.

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[1] See: http://www.intel.com/support/processors/pentiumpro/sb/CS-023719.htm
http://en.wikipedia.org/wiki/Pentium_Pro
http://developer.intel.com/design/chipsets/datashts/290523.htm

Examiner's Answer, paragraph bridging pages 7-8: ***On Whether Chen discloses a programmable error correcting circuit..***

In the paragraph bridging pages 7 and 8 of the Examiner's Answer the Examiner suggests that Chen meets the limitations of claims 3, 4, and 13.

Claims 3 and 13 set forth, *inter alia*:

> "a programmable error correcting circuit that receives error correcting information and processor instructions containing errors . . . wherein the error correcting information comprises a key which enables selection of error correction specific to an error correction scheme used to generate the errors.

Claim 13 further provides that "the instructions provided to said processor include an intentional introduction of errors which are correctable with error correction algorithms, said correction algorithms pre-selected according to the key."

The Examiner holds that "intentionally forced errors [inserted by the DIMM unit described in Chen] that the host computer system error control logic is capable of detecting and correcting . . . [meet] the limitation of an error correction algorithm." According to the Examiner, the intentional error forces a single bit error by inverting the logic state of a predetermined bit within the corrected data word . . . which would meet the limitation of the key to provide error correction. "Therefore," writes the Examiner, "inverting a single bit is the algorithm, and the predetermined bit is the key" (first full sentence, page 8 of the Examiner's Answer).

As Appellant understands the argument proffered by the Examiner, the "key" is the identity or bit number of the inverted bit. That is, if the predetermined bit is the least significant bit, then the identity of the least significant bit in the data word constitutes the key. However, there is no suggestion that the information as to which bit to invert is supplied to the error correcting circuit and stored in RAM on the same chip as the processing circuitry as required. Furthermore, the claim clearly requires that the error correcting circuit receives "error correcting information and processor instructions containing errors" and that "the programmable error correction generates corrected processor instructions in response to said processor instructions containing errors and said error correcting information" (claim 1, lines 12-13). The Examiner appears to be asserting that a single flipped bit satisfies the limitations of (1) the processor instruction containing an error (the error caused by the flipped bit), (2) the algorithm, and (3) the key. Appellant respectfully submits that these claim limitations should

be given their plain meaning, which is to say that each limitation refers to a distinct element of the invention, and cannot be met by a single flipped bit.

Furthermore, even if they were met by a single flipped bit, there is no suggestion in Chen of storing the identity of the predetermined bit in RAM on the same chip as the processing circuitry.

Examiner's Answer, page 8 lines 5-7: ***On whether Chen teaches a Microprocessor...***

The Examiner's brief remarks (page 8, lines 5-7 of the Examiner's Answer) in response to whether Chen shows a microprocessor do not address the core argument made in the Appeal Brief with regard thereto. The Examiner consistently confuses, to his own advantage, the ASIC chip described in Chen that has error correcting circuitry, and the "host computer system" which presumably has a processor unit, which may also have an error correction circuit (but is not described). The claimed invention is not a series of disconnected elements floating in space that the Examiner can identify anywhere in Chen and conclude that the invention was therefore anticipated. Rather, the invention as claimed includes a plurality of elements that interact and interoperate with each other in a specific manner. For anticipation, these interactions must be present in Chen as well as the elements themselves. *Diamond v. Diehr*, 450 U.S. 175, 188-89, 209 USPQ 1, 9 (1981). The purpose of the argument beginning on page 5 of the Appeal Brief is to point out that the error correction circuit described by Chen is not a processor. Chen does not teach a processor, but an error correction circuit that works with a processor. Of course, Appellant understands that a processor is mentioned by Chen, but this processor is not part of the invention described in any detail by Chen, but is merely an element that works with the invention of Chen.

Examiner's Answer, page 8, lines 9-15: ***On whether Chen discloses a* programmable *Error Correction Circuit...***

The Examiner suggests that, since "the error correcting logic of Chen has been programmed to detect and correct a specific type of error (i.e., inverted logic state of a predetermined bit" Chen therefore meets the limitation of "programmable error correcting circuitry" (see second full paragraph, page 8 of the Examiner's Answer). Appellant respectfully disagrees. "Programmable" and "programmed" are two different words having distinct meanings. An ASIC circuit may be designed using a programming language, and perhaps in that vague sense, be "programmed," but a hard-wired logic circuit relying on logic gates to carry out a fixed operation is most certainly not "programmable" when interpreted

according to its broadest reasonable interpretation consistent with the interpretation taken by those skilled in the art.

The Examiner further suggests that the claims do not require a positive programming step (page 8, second full paragraph of the Examiner's Answer). Perhaps not, but the claims do require that the error correcting circuit respond to the error correcting information, which may include a key (claim 3) which in effect *instructs* the circuit as to how to perform the error correction (claim 13). Claims 1, 3, 4, 13, and 14 are directed to an apparatus, not a method, and therefore a "positive programming step" is not required. The Examiner cannot simply read over the term "programmable" if it is inconvenient.

Examiner's Answer, page 8, lines 16-19: ***On whether Chen teaches error correcting circuit on the same chip as the microprocessor. . .***

The Examiner states that "Chen discloses that the error correction circuitry can also be implemented within a central processing unit." The Examiner is mistaken. Chen mentions that error correction circuits are known in processors, but *nowhere* does Chen suggest that the error correction circuit described with reference to the Figures "can also be implemented" in the CPU. The two units work together. As described in Chen, when the robust error correction circuit in the DIMM memory module identifies and corrects an error, it cannot be properly logged by the operating system because it is isolated from the operating system. To overcome this limitation, Chen deliberately inserts a simple error that *can* be identified and corrected by the processor. The error correction unit of the CPU therefore fixes the simple error, and raises an exception that can be logged by the operating system. See column 25, lines 4-46. There is no suggestion of implementing a robust error correction unit as described by Chen in the processor.

Examiner's Answer, paragraph bridging pages 8-9: ***On whether Chen shows selecting an error correction scheme based on error correction information...***

The Examiner suggests that since Chen has an internal signal that identifies whether an error is a single bit or a double bit error, Chen shows an error correction scheme based on error correction information. However, claim 1 requires that the "error correcting information" be stored on RAM on the processor chip; claim 17 includes "a memory location for storing error correction information," and claim 18 sets forth a method including "storing error correction control information on said chip." Chen doesn't mention storing the internal signal that identifies whether the error is a single bit or a double bit error on the processor chip or anywhere else.

Examiner's Answer, second full paragraph of page 9: ***On whether Chen shows intentionally placing errors in a computer program that is processed by a microprocessor...***

The Examiner asserts that Chen meets the limitation of intentionally inserting errors into a computer program that is processed by a microcomputer because,

> "intentionally inserted errors of Chen are inserted into read/write instructions (Col. 7, lines 1-22). Read/write instructions are a part of the operating system, which is a computer program. Therefore, Chen discloses placing errors in a computer program because the errors are inserted into the read/write instructions."

Appellant respectfully disagrees. First, Chen does not mention inserting errors into read/write instructions. In fact, the word "instruction" appears only once in the entire Chen reference, and that is in the first sentence of the fourth paragraph of the Summary. The portion of Chen identified by the Examiner, Col. 7, lines 1-22, refer to read and write *operations* performed by the ASIC chip on the DIMM memory module, not read and write instructions. The difference is this: A read instruction is a software instruction to read data whereas a read operation is the operation of carrying out the read instruction by hardware. Since read and write instructions are not altered by Chen, there is no showing by Chen of intentionally inserting errors into a computer program as set forth in claim 18.

For the reasons cited above and for other reasons cited in the Appeal Brief submitted October 17, 2006, Appellant respectfully submits that the present application is in condition for allowance and that the outstanding office action should be reversed.

Respectfully submitted,
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